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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/652,550	JONO ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	AU

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,11-19,21-32,62-66 and 69-80* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11-19,21-32,62-66 and 69-80* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 77 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 77, in lines 2-3, the phrase "the over-etching comprises varying at least one of the gases" fails to clarify what is the varying at least one of the gases?

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 69-71, 73 and 75 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,350,655 to Mizuo.

Regarding claim 69, Mizuo (figures 1A-7) teaches a method of forming an isolation trench in a semiconductor material comprising:

forming a masking layer (3) over a semiconductor substrate (1);

etching through the masking layer (3) and exposing an upper surface of the semiconductor substrate (1), the etching comprising over-etching through the upper surface of the semiconductor substrate (1) while some of the masking layer masks some of the substrate (1) to form a first isolation trench portion (4) within the semiconductor substrate (1), the first isolation trench portion (4) having a first depth within the semiconductor substrate (1) and having a first sidewall intersecting the upper surface of the semiconductor substrate (1) at a first angle (70^{o});

forming a second isolation trench portion (7) within the semiconductor substrate (1), the second isolation trench portion (7) being formed within and extending below the first isolation trench portion (4), the second isolation trench portion (7) having a second depth within the semiconductor substrate (1) and including a second sidewall intersecting the first sidewall at an angle (80^{o}-90^{o}) with respect to the upper surface that is greater than the first angle; and

filling the first (4) and second (7) isolation trench portions with dielectric material (10) (column 10, lines 3-8).

Regarding claim 70, Mizuo teaches the masking layer comprises a silicon nitride layer (3).

Regarding claim 71, Mizuo teaches the masking layer comprises an oxide layer (2).

Regarding claim 73, Mizuo teaches the over etching (forming first isolation trench portion [4]) comprises an environment of etch gases (column 8, lines 57-59), and forming of the second isolation trench portion (7) comprises a different environment of different etch gases (column 9, lines 41-44).

Regarding claim 75, Mizuo teaches the etching (etching the masking layer) and the over-etching (forming first isolation trench portion [4]) comprises a plasma environment of etch gases (column 8, lines 52-59).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,350,655 to Mizuo.

Regarding claim 1, Mizuo (figures 1A-7) teaches a method of forming an isolation trench in a semiconductor material comprising:

forming a first isolation trench portion (4) within a semiconductor material (1) with a first gas mixture (column 8, lines 57-59), the first isolation trench portion (4) having a first depth within the semiconductor material (1) and having a first sidewall intersecting a surface of the semiconductor material at a first angle (70^{o});

forming a second isolation trench portion (7) within the semiconductor material (1) with a second gas mixture (column 9, lines 41-44) different from the first gas mixture, the second isolation trench portion (7) being formed within and extending below the first isolation trench portion (4), the second isolation trench portion (7) having a second depth within the

semiconductor material (1) and including a second sidewall intersecting the first sidewall at an angle (80°-90°) with respect to the surface that is greater than the first angle; and

filling the first (4) and second (7) isolation trench portions with dielectric material (10) (column 10, lines 3-8).

Mizuo teach forming the first isolation trench portion (4) comprises forming the first isolation trench portion to have a first depth about 50 percent of a sum of the first and second depths within the semiconductor material (the depth of the first trench [4] is about 2000 Angstroms [column 9, lines 22-23]; the depth of the second trench [7] is about 2000 Angstroms [column 9, lines 59-60]; the total of [4] and [7] is about 4000 Angstroms [column 9, lines 60-62]).

Mizuo differs from the claimed invention by not showing the first isolation trench portion to have a first depth of between five and thirty percent of a sum of the first and second depths within semiconductor material. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the first isolation trench portion to have a first depth of between five and thirty percent of a sum of the first and second depths within semiconductor material because it reduces the size of the trench. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 2, Mizuo teaches forming the second isolation trench portion includes forming the second angle about 80°-90° (column 9, lines 50-51).

Regarding claim 3, Mizuo teaches forming the first isolation trench portion (4) includes forming the first angle about 70° (column 8, lines 57-64) and forming the second isolation trench portion (7) includes forming the second angle about 80°-90° (column 9, lines 50-51).

Regarding claim 4, Mizuo teaches the semiconductor material (1) comprises silicon (column 8, lines 40-41).

Regarding claim 12, Mizuo teaches forming the first isolation trench portion (4) comprises forming the first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment.

7. Claims 5, 13-17, 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,350,655 to Mizuo in view of US Patent No. 5,801,083 to Yu et al. and US Patent No. 6,380,095 to Liu et al.

Regarding claim 5, the disclosures of Mizuo are discussed as applied to claims 1-4 and 12 above.

Mizuo further teaches forming a silicon nitride layer (3) over the semiconductor material surface (1). Mizuo differs from the claimed invention by not showing forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls. However, Yu et al. (figure 1) teach forming a photoresist layer (4) on the silicon nitride layer (3). Therefore, it would have obvious to one having ordinary skill in the art at the time the invention was made for forming a photoresist layer on the silicon nitride layer because it prevents damage for below layer. The combined device show forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls.

Mizuo differs from the claimed invention by not showing plasma etching through the silicon nitride layer using plasma conditions that also deposit a polymer on the sidewalls; continuing the plasma etching for a predetermined time interval after the silicon nitride layer has been etched through and continuing to deposit polymer on the sidewalls to form the first isolation trench portion using the same plasma conditions; and stopping the etching and depositing at the end of the predetermined time interval. However, Yu et al. (figures 1-3) teach forming a polymer layer (6b) on the sidewall. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Yu et al. into the device taught by Mizuo because it eliminates the top corner wraparound and protects the sidewalls against an etching attack from the etching gas. The combined device show plasma etching through the silicon nitride layer using conditions that also deposit a polymer on the sidewalls; continuing etching for a predetermined time interval after the silicon nitride layer has been broached and continuing to deposit polymer on the sidewalls; and stopping the etching and depositing at the end of the predetermined time interval.

The combined device differs from the claimed invention by not showing the masking layer sidewalls. However, Liu et al. teach the masking layer sidewalls (column 13, lines 37-42). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate teaching of Liu et al. into the device taught by Mizuo and Yu et al. because it protects the sidewalls of the trench. The combined device shows the opening including masking layer sidewalls; plasma etching through the silicon nitride layer using plasma conditions that also deposit a polymer on the masking layer sidewalls and continuing the plasma etching for a predetermined time interval after the silicon nitride layer has been etched through

and continuing to deposit polymer on the masking layer sidewalls to form the first isolation trench portion using the same plasma conditions.

Regarding claim 13, the disclosures of Mizuo, Yu et al. and Liu et al. are discussed as applied to claim 5 above.

Mizuo, Yu et al. and Liu et al. differ from the claimed invention by not showing forming the first isolation trench portion comprises etching the first isolation trench portion using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 from 0.11 to 0.67. It would have been obvious to one having ordinary skill in the art at the time the invention was made for forming the first isolation trench portion comprises plasma etching the first isolation trench portion using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 = 0.11 to 0.67 because it reduces the size of the trench. Furthermore, it has been held that discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 14, the disclosures of Mizuo, Yu et al. and Liu et al. are discussed as applied to claim 13 above.

Regarding claim 15, Mizuo teaches forming the first isolation trench portion (4) comprises forming the first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment.

Regarding claim 16, the disclosures of Mizuo, Yu et al. and Liu et al. are discussed as applied to claim 13 above.

Regarding claim 17, the disclosures of Mizuo, Yu et al. and Liu et al. are discussed as applied to claim 13 above.

Regarding claim 19, the disclosures of Mizuo, Yu et al. and Liu et al. are discussed as applied to claim 13 above.

Regarding claim 21, the disclosures of Mizuo, Yu et al. and Liu et al. are discussed as applied to claim 13 above.

8. Claims 6, 7, 65 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuo and Yu et al. in view of Liu et al., and further in view of US Patent No. 6,383,931 to Flanner et al.

Regarding claim 6, the disclosures of Mizuo, Yu et al. and Liu et al. are discussed as applied to claim 5 above, the combined device further teach providing a mixture of gasses chosen from CF_4 and $CH F_3$ (Yu et al.; column 3, lines 10-11).

The combined device differs from the claimed invention by not showing supplying radio frequency excitation to the mixture. However, Flanner et al. teach radio frequency (column 11, lines 38-45). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Flanner et al. into the device taught by Mizuo, Yu et al. and Liu et al. because it is capable of withstanding the temperature and chemical environment of semiconductor manufacture.

Regarding claim 7, the disclosures of Mizuo, Yu et al., Liu et al. and Flanner et al. are discussed as applied to claim 6.

Regarding claims 65-66, the disclosures of Mizuo, Yu et al., Liu et al. and Flanner et al. are discussed as applied to claim 6 above.

9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuo in view of US Patent No. 6,258,688 to Tsai.

Regarding claim 8, the disclosures of Mizuo are discussed as applied to claims 1-4 and 12 above.

Mizuo differs from the claimed invention by not forming the first isolation trench portion comprises plasma etching the first isolation trench portion using gases including CF_4 and CHF_3. However, Tsai teaches forming the isolation trench portion comprises plasma etching using compound gases of CF_4 and CHF_3 (column 5, lines 18-38). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Tsai into the method taught by Mizuo because it reduces the size of the trench.

Mizuo and Tsai differ from the claimed invention by not showing forming the first isolation trench portion comprises plasma etching the first isolation trench portion using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 from 0.11 to 0.67. It would have been obvious to one having ordinary skill in the art at the time the invention was made for forming the first isolation trench portion comprises plasma etching the first isolation trench portion using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 = 0.11 to 0.67 because it reduces the size of the trench. Furthermore, it has been held that discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuo in view of US Patent No. 5,874,317 to Stolmeijer.

Regarding claim 11, the disclosures of Mizuo are discussed as applied to claims 1-4 and 12 above.

Mizuo differs from the claimed invention by not planarizing the dielectric material filling the first and second isolation trench portions. However, Stolmeijer teaches planarizing the surface of the insulating layer (see figure 22). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Stolmeijer into the method taught by Mizuo, since it reduces the size of the device. The combined device shows planarizing the dielectric material filling the first and second isolation trench portions.

11. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuo and Yu et al. in view of Liu et al., and further in view of US Patent No. 5,874,317 to Stolmeijer.

Regarding claim 18, the disclosures of Mizuo, Yu et al. and Liu et al. are discussed as applied to claims 5, 13-17 and 19-21 above.

The combined device differs from the claimed invention by not showing planarizing the dielectric material filling the first and second isolation trench portions. However, Stolmeijer teaches planarizing the surface of the insulating layer (see figure 22). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Stolmeijer into the method collectively taught by Mizuo, Yu et al. and Liu et al., since it reduces the size of the device. The combined device shows planarizing the dielectric material filling the first and second isolation trench portions.

12. Claims 22, 24, 27-30, 32 and 62-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,969,393 to Noguchi. in view of US Patent No. 6,274,457 to Sakai et al.

Regarding claim 22, Noguchi (figures 2A-4B) teaches a method of forming an isolation trench isolated transistor comprising:

forming first and second trenches disposed to a respective side of a portion of silicon (101), forming the first and second isolation trenches;

filling the first and second isolation trench portions with dielectric material (103);

forming a gate (108) extending across the silicon portion from the first isolation trench to the second isolation trench; and

forming source and drain regions (109) extending between the first and second isolation trench portions, the source region (109) being disposed adjacent one side of the gate (108) and the drain region (109) being disposed adjacent another side of the gate (109) that is opposed to the one side.

Noguchi differs from the claimed invention by not forming a mask on a surface of the portion of silicon, the mask including first and second openings corresponding to the first and second isolation trenches; forming a first isolation trench portion within the portion of silicon in each of the first and second openings, each first isolation trench portion having a first depth within the portion of silicon and having a first sidewall intersecting a surface of the portion of silicon at a first angle; and forming a second isolation trench portion within the portion of silicon and extending below each of the first isolation trench portions, the second isolation trench portions having a second depth within the portion of silicon and including a second sidewall

intersecting a respective one of the first sidewalls at an angle with respect to the surface that is greater then the first angle. However, Sakai et al. teach forming a mask (column 9, line 42) on the surface, the mask including an opening corresponding to the isolation trench; forming a first isolation trench portion (a trench portion that has an angle of A1) in the opening, the first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle; and forming a second isolation trench portion (a trench portion that has an angle of A2) within and extending below the first isolation trench portion (a trench portion that has an angle of A1), the second isolation trench portion (a trench portion that has an angle of A2) having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater then the first angle (see figures 7, 8a-d; column 9, line 25 – column 10, line 13).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the trench-forming method of Sakai et al. into the first and second isolation trench-forming methods of Noguchi because it provides good electrical characteristics to the device isolation region. The combined device show forming a mask on the surface, the mask including an opening corresponding to the isolation trench; forming a first isolation trench portion within the portion of silicon in the opening, the first isolation trench portion having a first depth within the portion of silicon and having a first sidewall intersecting a surface of the portion of silicon at a first angle; and forming a second isolation trench portion within the portion of silicon and extending below the first isolation trench portion, the second isolation trench portion having a second depth within the portion of silicon and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is

greater then the first angle, the second isolation trench portion having a bottom portion of silicon at the second depth; doping the bottom portion of the second isolation trench portion.

Regarding claim 24, Noguchi teaches forming a silicon nitride layer (102) over the silicon surface (101). Noguchi differs from the claimed invention by not showing forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls. However, Sakai et al. (figure 9a) teach forming a masking layer (104) on atop the silicon nitride layer (103). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sakai et al. into the device taught by Noguchi because it protects and prevents damage for below layer.

Regarding claim 27, the combined device teaches forming a first isolation trench portion comprises forming a first isolation trench portion having a first sidewall intersecting a surface of the portion of silicon at an angle in a range of from about thirty degrees to about seventy degrees (Sakai et al.).

Regarding claim 28, the combined device teaches forming the first isolation trench portion comprises forming the first isolation trench portion including a side at least some of which forms a substantially straight linear segment.

Regarding claim 29, the combined device teaches forming the second isolation trench portion comprises forming the second isolation trench portion having a second sidewall forming an angle of more than eighty degrees with the surface (Sakai et al.).

Regarding claim 30, the combined device teaches forming the first isolation trench portion (Sakai et al.; a trench portion that has angle of A1) comprises forming the first isolation trench portion having a first depth about 3.75 to 37.5 percent of a sum of the first and second depths

within the portion of silicon (the depth of the first trench is about 30-300 nm [column 9, lines 43-44]; the depth of the second trench is about 50-500 nm [column 9, lines 60-62]; the total of first and second trench is about 80-800 nm). The combined device shows the first isolation trench portion having a first depth of between five and fifty percent of a sum of the first and second depths within the portion of silicon.

Regarding claim 32, the combined device teaches a gate comprising polysilicon ([108] of Noguchi).

Regarding claim 62, the combined device teaches the source region (Noguchi; [109]) is disposed adjacent only one side of the gate.

Regarding claim 63, the combined device teaches the drain region (Noguchi; [109]) is disposed adjacent only one side of the gate.

Regarding claim 64, the combined device teaches the source region and drain region (Noguchi; [109]) are disposed directly opposite one another on opposite sides of the gate.

13. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi and Sakai et al., and further in view of US Patent No. 6,258,688 to Tsai.

Regarding claim 23, the disclosures of Noguchi and Sakai et al. are discussed as applied to claims 22, 24, 27-30, 32 and 62-64 above.

The combined device teaches forming the first isolation trench portion (a trench portion that has an angle of A1) comprises etching the silicon surface. Noguchi and Sakai et al. differ from the claimed invention by not etching the silicon surface using gases including CF_4 and CHF_3 to form the first isolation trench portion. However, Tsai teaches forming the isolation

trench portion comprises plasma etching using compound gases of CF_4 and CHF_3 (column 5, lines 18-38). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Tsai into the method taught by Noguchi and Sakai et al. because it reduces the size of the trench.

Noguchi, Sakai et al. and Tsai differ further from the claimed invention by not forming the first isolation trench portion comprises plasma etching the silicon surface using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 from 0.11 to 0.67. It would have been obvious to one having ordinary skill in the art at the time the invention was made to find the optimal ratio of the gases of CF_4 and CHF_3 because it reduces the size of the trench. Furthermore, it has been held that discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

14. Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi in view of Sakai et al., and further in view of US Patent No. 5,801,083 to Yu et al.

Regarding claim 25, Noguchi (figures 2A-4B) teaches a method of forming an isolation trench isolated transistor comprising:

forming first and second trenches disposed to a respective side of a portion of silicon (101), forming the first and second isolation trenches;

filling the first and second isolation trench portions with dielectric material (103);

forming a gate (108) extending across the silicon portion from the first isolation trench to the second isolation trench; and

forming source and drain regions (109) extending between the first and second isolation trench portions, the source region (109) being disposed adjacent one side of the gate (108) and the drain region (109) being disposed adjacent another side of the gate (109) that is opposed to the one side.

Noguchi differs from the claimed invention by not forming an oxide layer over the surface of the portion of silicon, the oxide layer including first and second openings corresponding to the first and second isolation trenches; forming a first isolation trench portion within the portion of silicon in each of the first and second openings, each first isolation trench portion having a first depth within the portion of silicon and having a first sidewall intersecting a surface of the portion of silicon at a first angle; and forming a second isolation trench portion within the portion of silicon and extending below each of the first isolation trench portions, the second isolation trench portions having a second depth within the portion of silicon and including a second sidewall intersecting a respective one of the first sidewalls at an angle with respect to the surface that is greater then the first angle. However, Sakai et al. teach forming an oxide layer (5) over the surface of the portion of silicon (1), the oxide layer (5) including an opening corresponding to the isolation trench; forming a first isolation trench portion (a trench portion that has an angle of A1) in the opening, the first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle; and forming a second isolation trench portion (a trench portion that has an angle of A2) within and extending below the first isolation trench portion (a trench portion that has an angle of A1), the second isolation trench portion (a trench portion that has an angle of A2) having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is

greater then the first angle (see figures 7, 8a-d; column 9, line 25 – column 10, line 13). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the trench-forming method of Sakai et al. into the first and second isolation trench-forming methods of Noguchi because it provides good electrical characteristics to the device isolation region.

Noguchi and Sakai et al. differ from the claimed invention by not showing plasma etching through the oxide layer using conditions that also deposit a polymer on the sidewalls; continuing plasma etching for a predetermined time interval after the oxide layer has been broached and continuing to deposit polymer on the sidewalls to form the first isolation trench portion using the same plasma conditions; and stopping the etching and depositing at the end of the predetermined time interval. However, Yu et al. (figures 1-3) teach forming a polymer layer (6b) on the sidewall. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Yu et al. into the device taught by Mizuo because it eliminates the top corner wraparound and protects the sidewalls against an etching attack from the etching gas. The combined device show plasma etching through the oxide layer using conditions that also deposit a polymer on the sidewalls; continuing plasma etching for a predetermined time interval after the silicon nitride layer has been broached and continuing to deposit polymer on the sidewalls to form the first isolation trench portion using the same plasma conditions; and stopping the etching and depositing at the end of the predetermined time interval.

Regarding claim 26, Yu et al. teach etching using gases including CF_4 and CHF_3 (column 3, lines 5-12). Noguchi, Sakai et al. and Yu et al. differ from the claimed invention by not

showing etching using gases including CF_4 and CHF_3 in a ration of CF_4/CHF_3 = 0.11 to 0.67. It would have been obvious to one having ordinary skill in the art at the time the invention was made for etching using gases including CF_4 and CHF_3 in a ration of CF_4/CHF_3 = 0.11 to 0.67 because it reduces the size of the trench. Furthermore, it has been held that discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

15. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi and Sakai et al., and further in view of US Patent No. 5,874,317 to Stolmeijer.

Regarding claim 31, the disclosures of Noguchi and Sakai et al. are discussed as applied to claims 22-24, 27-30, 32 and 62-64 above.

Noguchi and Sakai et al. differ from the claimed invention by not planarizing the dielectric material filling the first and second isolation trench portions. However, Stolmeijer teaches planarizing the surface of the insulating layer (see figure 22). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Stolmeijer into the method taught by Noguchi and Sakai et al., since it reduces the size of the device. The combined device shows planarizing the dielectric material filling the first and second isolation trench portions.

16. Claim 72 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuo.

Regarding claim 72, Mizuo differs from the claimed invention by not showing the etching and over etching of etch gases with respective ratios of component gases. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the etching

and over etching of etch gases with respective ratios of component gases because it reduces the size of the trench. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

17. Claims 76-78 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuo in view of US Patent No. 5,801,083 to Yu et al.

Regarding claim 76, Mizuo differs from the claimed invention by not showing the etching and the over-etching comprises an environment of at least CF_4, CHF_3 and argon. However, Yu et al. teach etching using CF_4, CHF_3 and argon (column 3, lines 10-12). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Yu et al. into the method taught by Mizuo because it reduces the size of the trench. The combined device shows the etching and the over-etching comprises an environment of at least CF_4, CHF_3 and argon.

Regarding claim 77, the combined device shows the etching comprises an environment of at least CF_4 and CHF_3 (Yu et al.).

Regarding claim 78, the combined device shows the etching comprises an environment of at least CF_4 and CHF_3 gases (Yu et al.), and the over-etching comprises varying at least the CF_4 and CHF_3 gases (Mizuo; HBr and chlorine gases).

18. Claim 74 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuo in view of US Patent No. 6,342,428 to Zheng et al.

Regarding claim 74, Mizuo differs from the claimed invention by not showing terminating the forming of the second isolation trench portion; and de-chucking the semiconductor substrate in an environment of argon. However, Zheng et al. teach forming the isolation trench portion and de-chucking the semiconductor substrate from the etchant gases environment (column 6, line 52 – column 7, line 5). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Zheng et al. in the method taught by Mizuo because it provides a completed process of forming isolation trench in the semiconductor substrate. The combined device shows terminating the forming of the second isolation trench portion; and de-chucking the semiconductor substrate in an environment of argon.

19. Claim 79 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuo.

Regarding claim 79, Mizuo (figures 1A-7) teaches a method of forming an isolation trench in a semiconductor substrate comprising:

forming a masking layer (3) over a semiconductor substrate (1);

etching through the masking layer (3) and exposing an upper surface of the semiconductor substrate (1), the etching comprising an environment of etch gases (column 8, lines 52-54).

etching through the upper surface of the semiconductor substrate (1) to from a first isolation trench portion (4) within the semiconductor substrate (1), the etching comprising the etch gases (column 8, lines 57-59), the first isolation trench portion (4) having a first depth within the semiconductor substrate (1) and having a first sidewall intersecting the upper surface of the semiconductor substrate (1) at a first angle (70°);

etching a second isolation trench portion (7) within the semiconductor substrate (1), the second isolation trench portion (7) being formed within and extending below the first isolation trench portion (4), the second isolation trench portion (7) having a second depth within the semiconductor substrate (1) and including a second sidewall intersecting the first sidewall at an angle (80°-90°) with respect to the upper surface that is greater than the first angle; and

filling the first (4) and second (7) isolation trench portions with dielectric material (10) (column 10, lines 3-8).

Mizuo differs from the claimed invention by not showing the etching comprising an environment of etch gases with respective ratios of gases. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the etching comprising an environment of etch gases with respective ratios of gases because it reduces the size of the trench. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

20. Claim 80 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuo in view of US Patent No. 5,801,083 to Yu et al.

Regarding claim 80, the disclosures of Mizuo are discussed as applied to claim 79 above.

Mizuo differs from the claimed invention by not showing the etch gases of the environment comprises at least CF_4, CHF_3 and argon. However, Yu et al. teach etching using CF_4, CHF_3 and argon (column 3, lines 10-12). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of

Yu et al. into the method taught by Mizuo because it reduces the size of the trench. The combined device shows the etch gases of the environment comprises at least CF_4, CHF_3 and argon.

Response to Arguments

Applicant's arguments with respect to claims 1-8, 11-19, 21-32, 62-66 and 69-80 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
May 11, 2004

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